Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-18. (Canceled).

19. (Currently amended) A method of measuring an uncertainty window within which a target clock signal on a microprocessor die makes state transitions, the method comprising:

generating on the microprocessor die a first and second reference clock signals having the same frequency but differing in phase relationship;

defining a time window between features of the first and second reference clock signals;

comparing on the microprocessor die a plurality of cycles of the target clock signal to the reference clock signals to determine whether the target clock signal makes state transitions within the time window;

adjusting the time window; and

repeating the comparing ~~step~~ and adjusting ~~step~~ to determine the uncertainty window.

20. (Original) The method of measuring an uncertainty window as defined in claim 19 wherein generating the first and second reference clock signal on the microprocessor die further comprises:

coupling a core clock signal to a first adjustable delay chain;

delaying the core clock by a first length of time with the first adjustable delay chain to create the first reference clock signal;

coupling the core clock signal to a second adjustable delay chain; and

delaying the core clock by a length of time greater than the first length of time with the second adjustable delay chain to create the second reference clock signal.

21.-22. (Canceled).

23. (Original) The method of measuring an uncertainty window as defined in claim 19 wherein defining the time window further comprises defining the time window between corresponding low voltage to high voltage state transitions of the first and second reference clock signals.

24. (Original) The method of measuring an uncertainty window as defined in claim 19 wherein adjusting the time window further comprises adjusting the phase relationship of the first and second reference clock signals.

25.-26. (Canceled).

27. (Currently amended) A system for measuring an uncertainty window of a target clock signal of a microprocessor, the system comprising:

a measurement circuit on the die of the microprocessor;

an external measurement system coupled the measurement circuit by way of a scan chain of the microprocessor, and wherein the external measurement system executes software ~~adapted to control~~ that controls the measurement circuit through the scan chain;

wherein the external measurement system ~~is further adapted to adjust~~ adjusts a phase relationship of a plurality reference clock signals having varying phase, the plurality of reference clock signals define a plurality of time windows between corresponding features; and

wherein the measurement circuit compares the target clock signal to the plurality of time windows to determine the uncertainty window of the target clock signal.

28. (Original) The system for measuring the uncertainty window as defined in claim 27 wherein the measurement circuit further comprises:

a plurality of delay units each coupled to a host clock and creating the plurality of reference clock signals by selectively phase delaying the host clock signal by each of the delay units; and

a measurement unit coupled to the plurality of reference clock signals and the target clock signal, and wherein the measurement unit compares the plurality of reference clock signals to the target clock signal to determine the uncertainty window.

29.-31. (Canceled).

32. (Currently amended) The system for measuring the uncertainty window as defined in claim 27 wherein the external measurement system further comprises a microcontroller adapted to execute software algorithms coupled to the measurement circuit by way of the scan chain.

33. (Currently amended) In a system for measuring on the die of the electronic device an uncertainty window within which a target clock signal may make a state transition, a method of calibrating a measurement circuit comprising:

generating a first and second calibration signal, each calibration signal having the same frequency, but differing in phase relationship by a known period of time;

phase locking an output signal of a programmable delay chain to the first calibration signal;

noting a number of programmable taps required to phase lock to the first calibration signal;

phase locking the output signal of the programmable delay chain to the second calibration signal;

noting the number of programmable taps required to phase lock to the second calibration signal;

attributing the difference in the number of taps to lock to the first and second calibration signal to the known period of time; and thereby

attributing to each tap a portion of the known period of time.

34. (Original) The method of calibrating a measurement circuit as defined in claim 33 wherein generating the first and second calibration signal further comprises:

applying a host clock signal to a first delay element having known propagation delay to create the first calibration signal; and

applying the first calibration signal to a second delay element having known propagation delay to create the second calibration signal.

35.-44. (Canceled).

45. (Currently amended) A method for determining an uncertainty window within which a target clock signal of an electronic device makes state transitions, the method comprising:

generating on a microprocessor die a first, second, third and fourth reference clock signals having the same frequency but differing in phase relationship;

defining a first time bin between respective features of the first and second reference clock signals, defining a second time bin between respective features of the second and third reference clock signals, and defining a third time bin between respective features of the third and fourth reference clock signals;

comparing on the microprocessor die a plurality of cycles of the target clock signal to the reference clock signals to determine in which bin the target clock signal makes it state transitions;

adjusting the phase relationship of at least one of the reference clock signals, and thereby adjusting the time width of at least one time bin; and

repeating the adjusting ~~step~~ and the comparing ~~step~~ until the uncertainty window is determined.

46.-48. (Canceled).

49. (Original) The method of measuring an uncertainty window as defined in claim 45 wherein defining the time window further comprises defining the time window between corresponding low voltage to high voltage state transitions of the first and second reference clock signals, second and third reference clock signals, and the third and fourth reference clock signals.

50. (Currently amended) The method of measuring an uncertainty window as defined in claim 45 wherein adjusting the time bins further comprises adjusting the phase relationship of at least one of the first, second, third ~~and~~ or fourth reference clock signals.

51.-61. (Canceled).

62. (New) A method comprising:

generating on a microprocessor die a first and second reference clock signals having the same frequency but differing in phase relationship;

defining a time window between features of the first and second reference clock signals;

comparing on the microprocessor die a plurality of cycles of a target clock signal to the reference clock signals to determine whether the target clock signal makes state transitions within the time window;

adjusting the phase of only one of the first and second reference clock signals to adjust the time window; and

repeating the comparing and adjusting to determine an uncertainty window within which the target clock makes state transitions.

63. (New) A method comprising:

comparing within an electronic device a plurality of cycles of a target clock signal to a first and second reference clock signals to determine whether the target clock signal makes state transitions within a time window between features of the reference clock signals;

adjusting the phase of the first and second reference clock signals, wherein phases of the plurality of reference clock signals are independently controlled; and

repeating the comparing and independently adjusting to determine an uncertainty window within which the target clock on the electronic device makes state transitions.

64. (New) The method as defined in claim 63 further comprising:

generating the first and second reference clock signals within the electronic device;

phase delaying the second reference clock signal more than the first reference clock signal; and

defining the time window between features of the first and second reference clock signals.

65. (New) A system comprising

a clock domain region of an electronic device; and

a jitter measurement circuit comprising

a plurality of delay units creating a plurality of reference clock signals having the same frequency but differing in phase

relationship, wherein the phase delay of each reference clock signal is independently controlled; and

a measurement unit coupled to the plurality of reference clock signals and a target clock, wherein the measurement unit compares the target clock to the plurality of reference clock signals to determine an uncertainty window within which the target clock makes state transitions.

66. (New) The system as defined in claim 65 wherein each of the plurality of delay units couples to a scan chain, and wherein an external device controls the phase delay created by each delay unit by communicating with each delay unit over the scan chain.